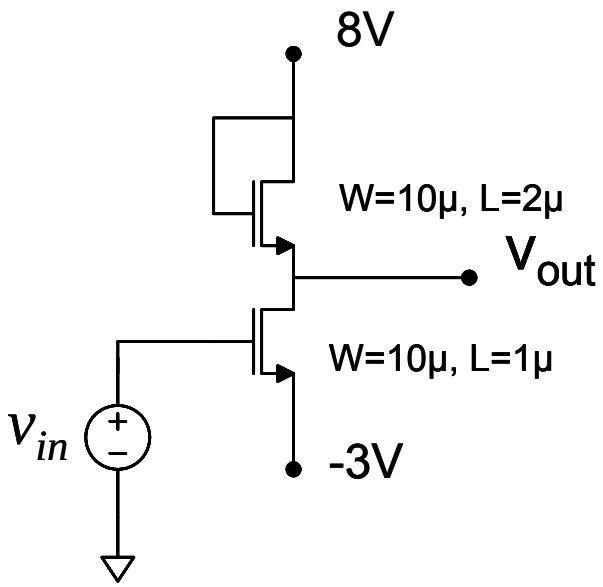
EE 333 Name _____
Final Exam - 2 hours (an additional 2 hours if needed)
Summer 2003

Instructions: The points allocated to each problem are as indicated. Students are permitted to bring up to 3 sheets of paper with any notes they deem appropriate. All work and answers should be written on the exam sheet itself. Unless specifically stated to the contrary, assume all operational amplifiers are ideal , all MOS transistors are from a process with $u_nC_{OX} = 100ua/v^2$, $V_{TN} = - V_{TP} = 1V$, $u_p=u_n/3$, $\lambda = 0$ and $\gamma =0$ and all bipolar transistors are from a process with $I_S = 10^{-15}A$, $\beta =100$ and $V_{AF} = \infty$.

If logic circuits are considered, assume the logic gates are designed in a process where the minimum length and width of the devices is 0.2u, $uCox = 100uA/v^2$ and $Cox = 5fF/u^2$. Define T_{REF} to be the sum of t_{HL} and t_{LH} for a reference inverter (with minimum-sized n-channel devices) driving an identical device that is sized for equal rise and fall times. Define C_{REF} to be the input capacitance to the reference inverter and assume $u_n/u_p =3$.

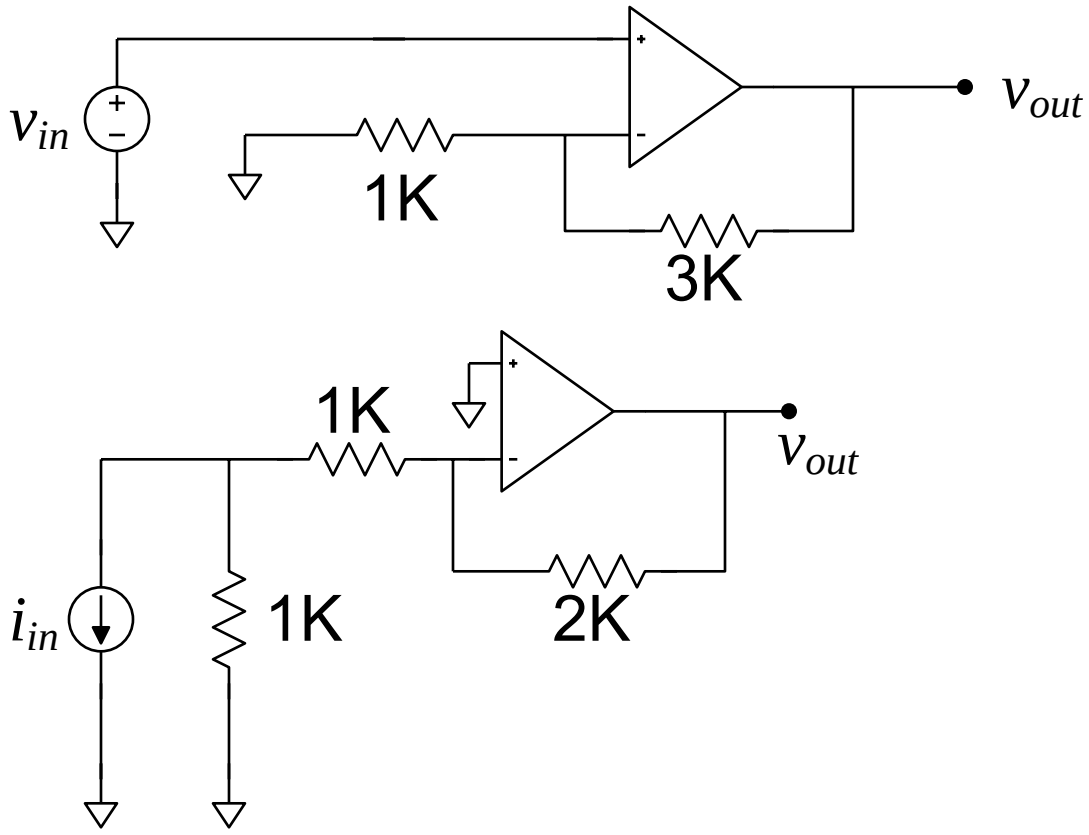
Problem 1 (10 pts). Determine V_{OUTQ} and $A_V=v_{out}/v_{in}$ for the circuit shown..



Problem 2 (10 pts) For the following circuits:

a) Determine the output variables indicated if the Op Amp is ideal

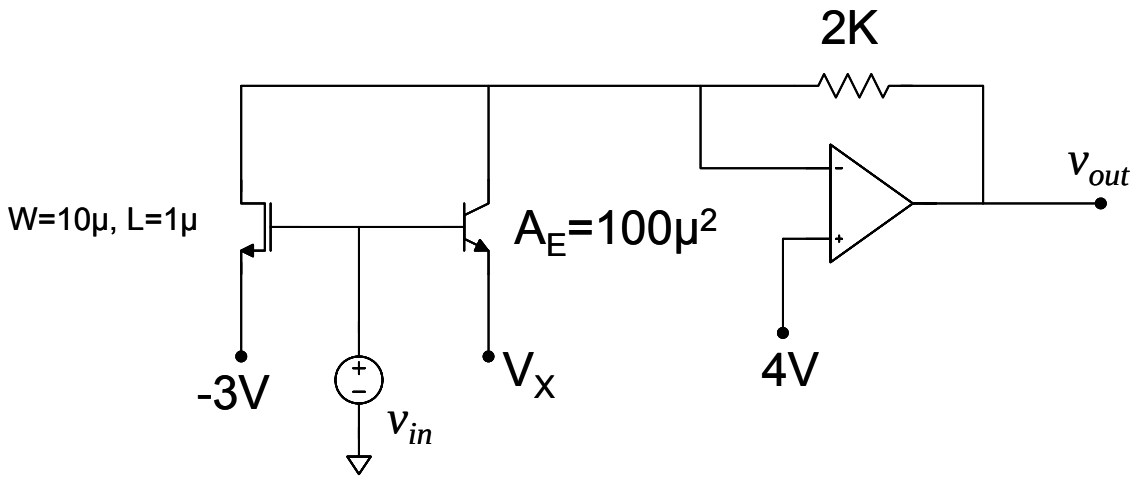
b) Determine the 3dB bandwidth in Hz of the amplifiers shown if the GB of the Op Amp is 3MHz.



Problem 3 (10 pts) For the circuit shown, assume V_X has been chosen so that the quiescent current in the collector of the BJT is 1mA.

a) Determine the quiescent output voltage

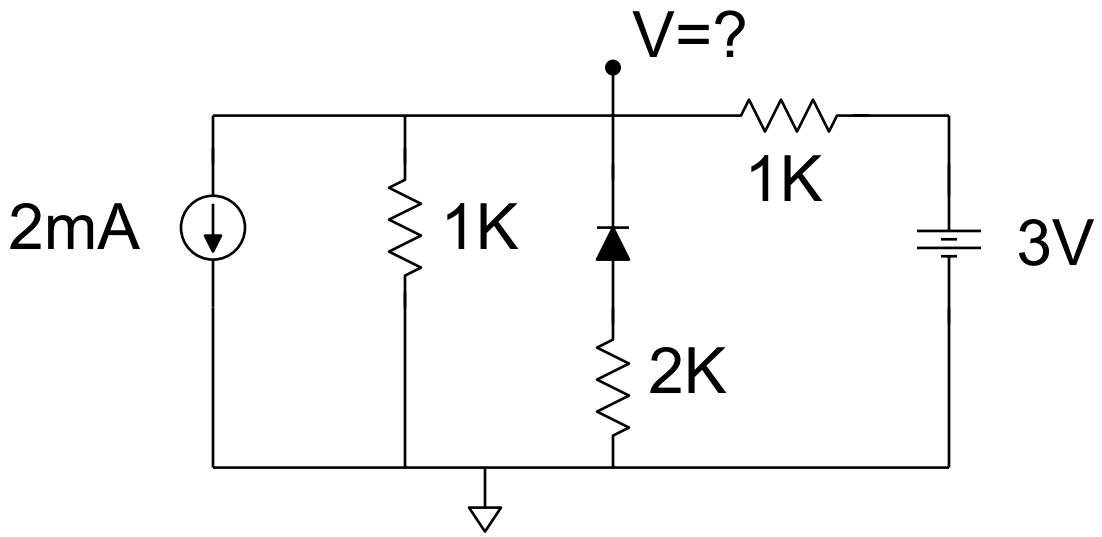
b) Determine the small signal voltage gain $A_v = v_{out}/v_{in}$.

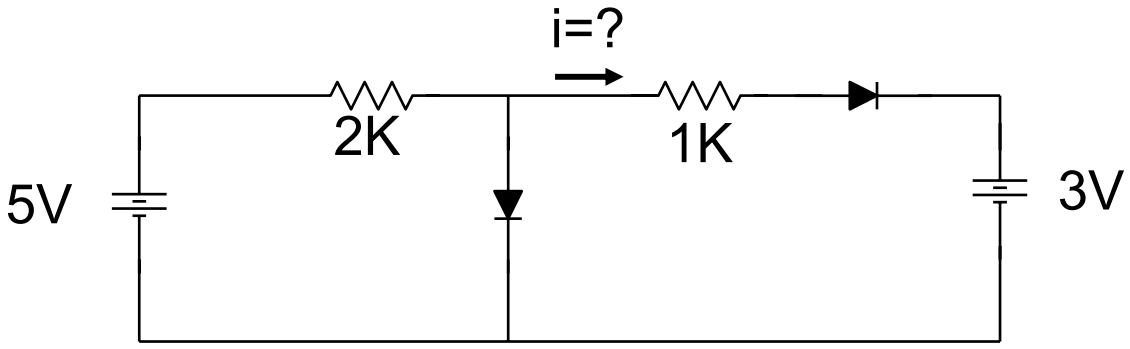


Problem 4 (10 pts) Assume a voltage amplifier has a frequency dependent gain given by the expression $A)s) = -\frac{4x10^6}{(s+400)(s+1200)}$

a) Determine the dc gain of the amplifier
b) Determine the 3dB bandwidth
c) Determine the poles of the amplifier
d) Determine the sinusoidal steady-state response if the input to the amplifier is given by the expression $V_{in}(t)$=.03sin600t

Problem 5 (10 pts) Determine the output variables indicated. Assume the diodes are ideal.



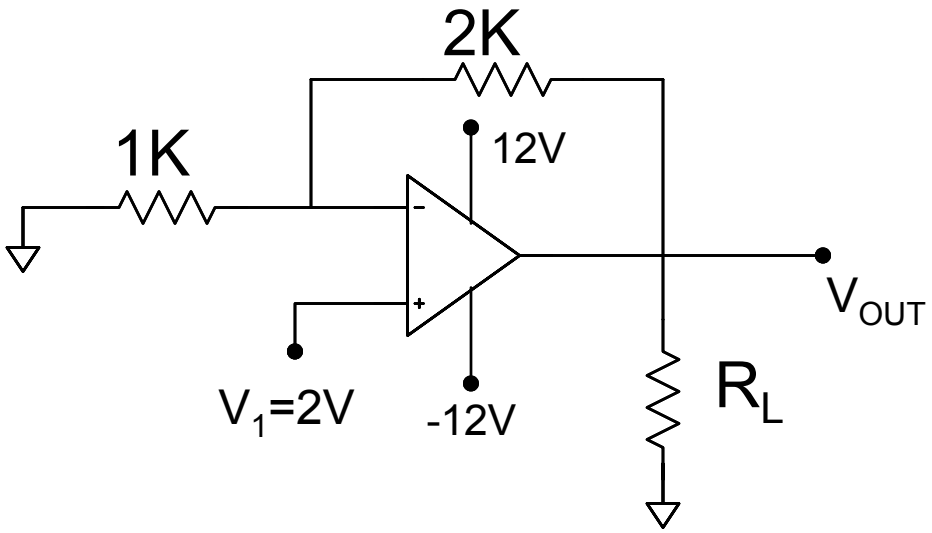


Problem 6 (10 pts) Assume the Op Amp is a rail to rail device (its output can swing to the positive and negative bias voltages) and that I_{OMAX}=15mA.

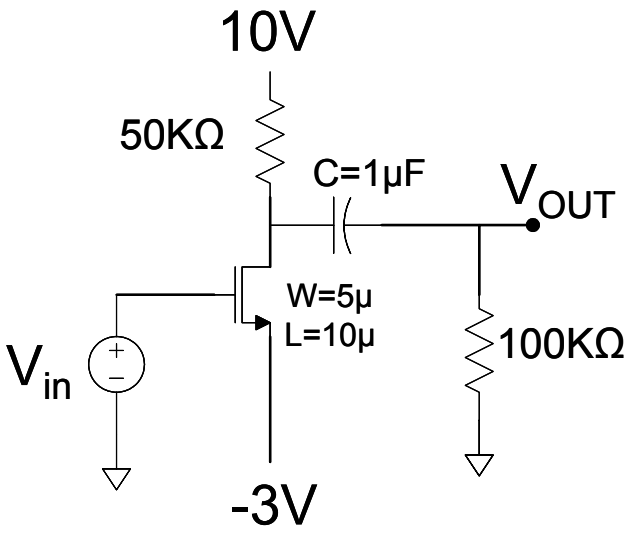
a) Determine V_{OUT} if R_L=2K

b) Determine V_{OUT} if R_L=0.25K

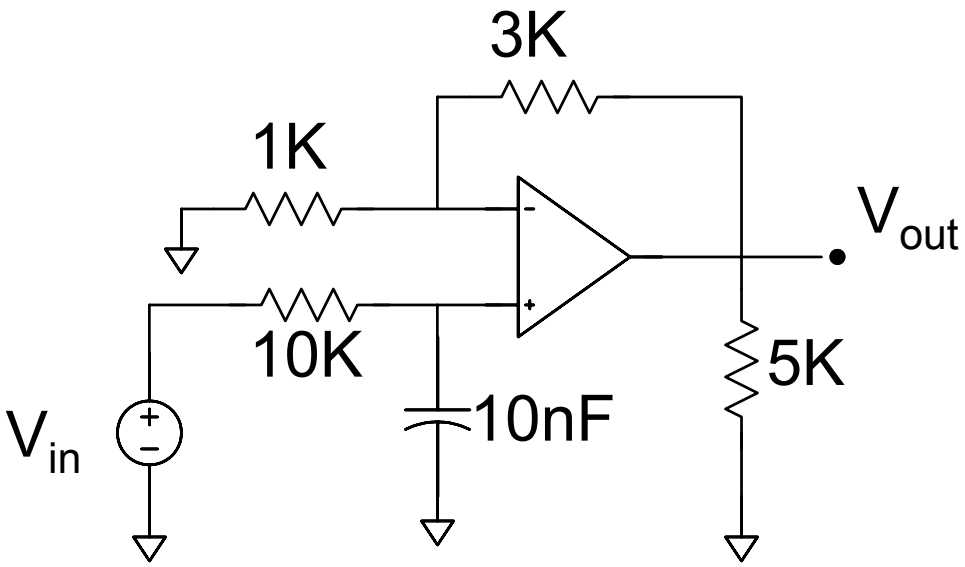
c) Determine V_{OUT} if R_L=2K and V_1 is increased to 5V.



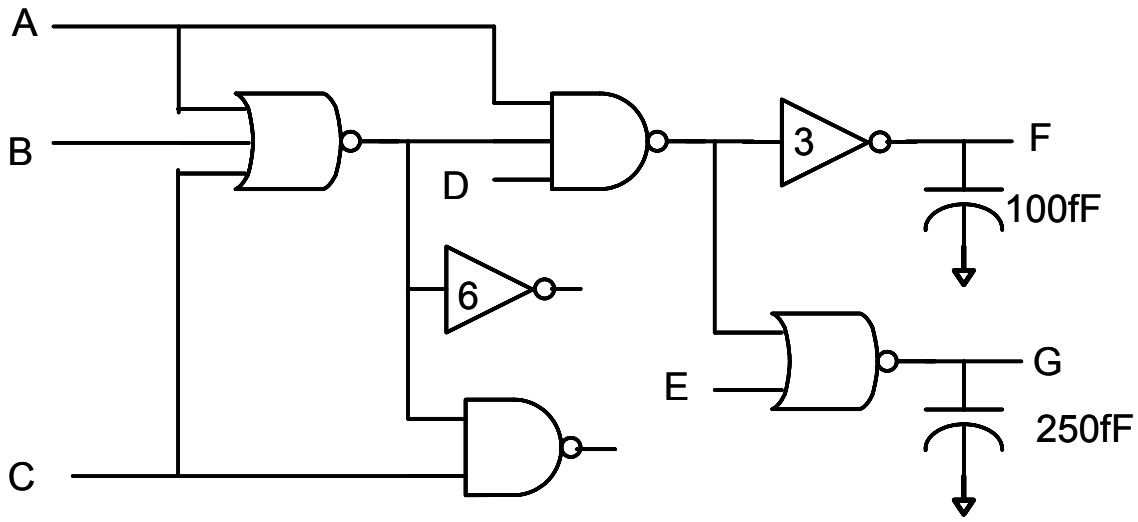
Problem 7 (10 pts) Determine the quiescent output voltage and the small signal voltage gain for the amplifier shown. .



Problem 8 (10 pts) Determine the steady state output voltage if Vin=0.1sin5000t



Problem 9 (10 pts) Determine the propagation delay for a signal to propagate from B to F. Assume all gates sized for equal rise and fall times and that the overdrive factors for each gate are as indicated by the number on the gate. If no number is shown, assume the overdrive factor is 1.



Problem 10 (10 pts) Implement the following Boolean functions at the transistor level with as few devices as possible in a) Static CMOS, b) PTL, and c) Complex Logic Gates. Assume the Boolean Variables A,B and C are available as inputs.

$$F = (\overline{A} + C) \bullet (A \oplus \overline{B})$$